Name & Std. No.: Riley Lawson 116555487 Lab Section: 6

Date: 11/12/2020

**Submission Instructions:**

**Prelab:**

1. **Complete the prelab**
2. **Submit this report with the prelab completed to Canvas before your lab starts**

**Lab:**

1. **Complete the lab according to the instructions**
2. **Take screenshots of your ModelSim waveform (note: to receive points your NetID has to be present in the screenshot) and insert them into this document.**
3. **Include screenshots of any related block design files or Verilog files in the report**
4. **Complete this report and reupload it to Canvas**

**PRELAB:**

*Complete the prelab and make sure you have your designs and circuit diagrams ready before the lab session. You may refer to your text book, Chapter 6.*

**Q1.** Design a simple counting device (Section 2.0).

Number of States: 6

Number of State Variables: 4

**State Table: State-Assigned Table:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Present State | Next State | | Output |  | Present State | Next State | | Output |
| w=0 | w=1 |  | w=0 | w=1 |  |
| A | A | B | 0 |  | 000 | 000 | 001 | 000 |
| B | B | C | 1 |  | 001 | 001 | 010 | 001 |
| C | C | D | 2 |  | 010 | 001 | 100 | 010 |
| D | D | E | 3 |  | 011 | 001 | 100 | 011 |
| E | E | F | 4 |  | 100 | 100 | 101 | 100 |
| F | F | A | 5 |  | 101 | 101 | 000 | 101 |

Canonical SOP Expressions for Next State Logic:

Y0 = !w!y1!y0 + !w!y2!y0 + w!y1!y0 + w!y2!y0

Y1 = !w!y2!y1y0 + w!y2y1 + !y2y1!y0

Y2 = !w!y2!y1y0 + y2!y1!y0 + wy2!y1

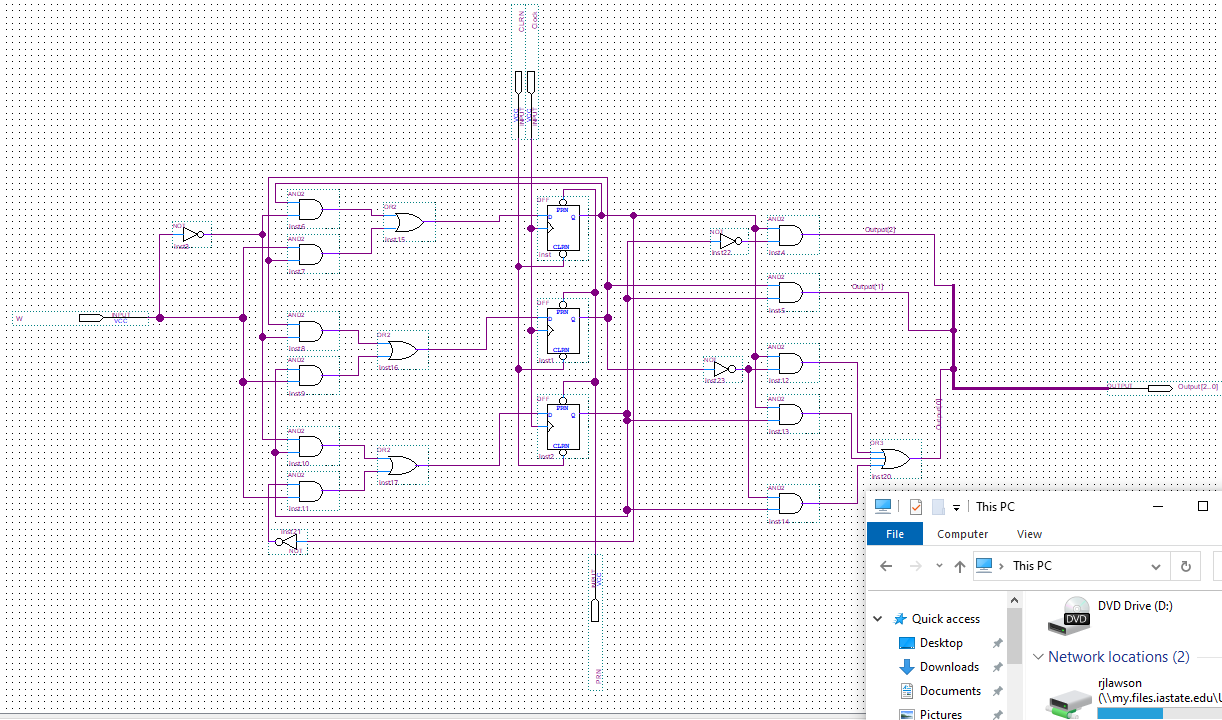
Simplified Next State Logic Expressions:

Y0 = w XOR y0

Y1 = wy0 XOR y1

Y2 = wY0Y! XOR y2

Circuit Diagram:



**Q2.** Design a simple counter (Section 3.0).

Number of States: 4

Number of State Variables: 5

**State Table: State-Assigned Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| Present State | Next State | | Output |
| w=0 | w=1 |
| A | A | B | 0 |
| B | B | C | 2 |
| C | C | D | 4 |
| D | D | A | 5 |

|  |  |  |  |
| --- | --- | --- | --- |
| Present State | Next State | | Output |
| w=0 | w=1 |
| 000 | 000 | 010 | 000 |
| 010 | 010 | 100 | 010 |
| 100 | 100 | 101 | 100 |
| 101 | 101 | 000 | 101 |

Canonical SOP Expressions for Next State Logic:

Y1 = !Q1wQ0 + Q1!w!Q0

Y2 = !wQ0 + w!Q0

Simplified Logic Expressions:

Y1 = Q1 XOR wQ0

Y2 = !wQ0 XOR Q0

Next State Logic Verilog Code:

module circuit\_nsl(w, Q1, Q0, Y1, Y0);

input w, Q1, Q0;

output Y1, Y0;

assign Y0 = w ^ Q0;

assign Y1 = Q1 ^ (w & Q0);

endmodule

Output Logic Verilog Code:

module circuit\_ol(Q1, Q0, Z2, Z1, Z0);

input Q1, Q0;

output reg Z2, Z1, Z0;

always @(Q1 or Q0)

begin

case({Q1,Q0})

2’b00: {Z2, Z1, Z0} = 3; b000;

2’b01: {Z2, Z1, Z0} = 3; b010;

2’b10: {Z2, Z1, Z0} = 3; b100;

2’b11: {Z2, Z1, Z0} = 3; b101;

endcase

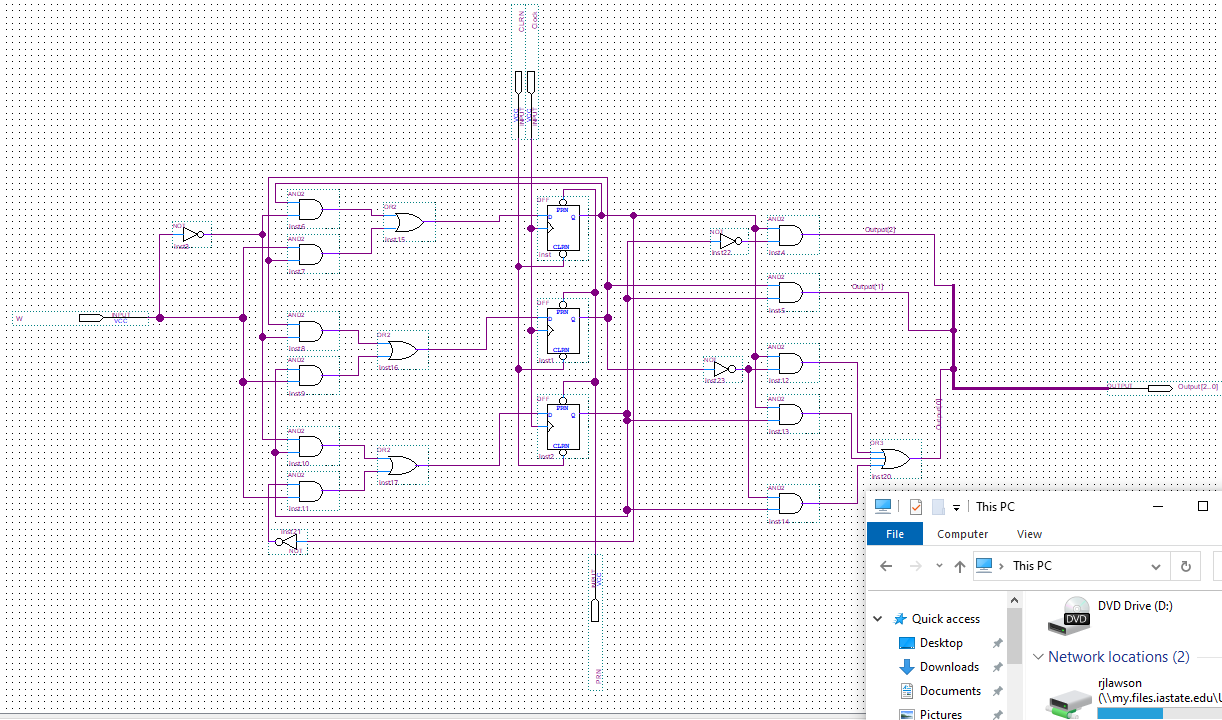
endmodule

**LAB:**

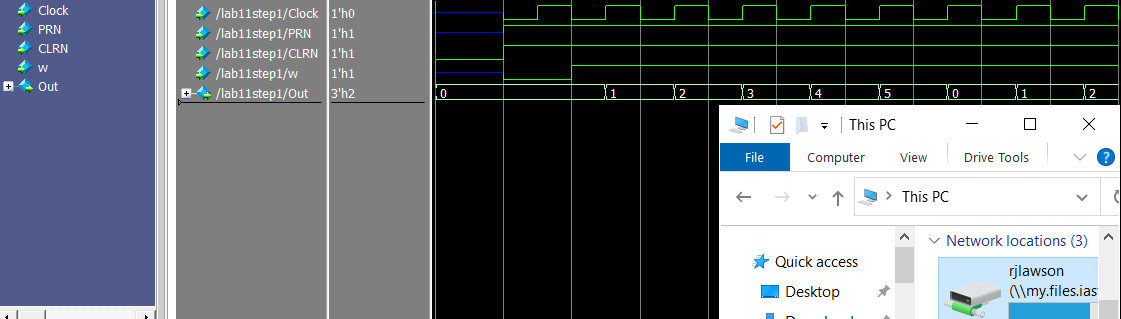
**2.0 A Simple Counting Device**

Screenshots:

<<<Insert a screenshot of your module-6 counter BDF here>>>



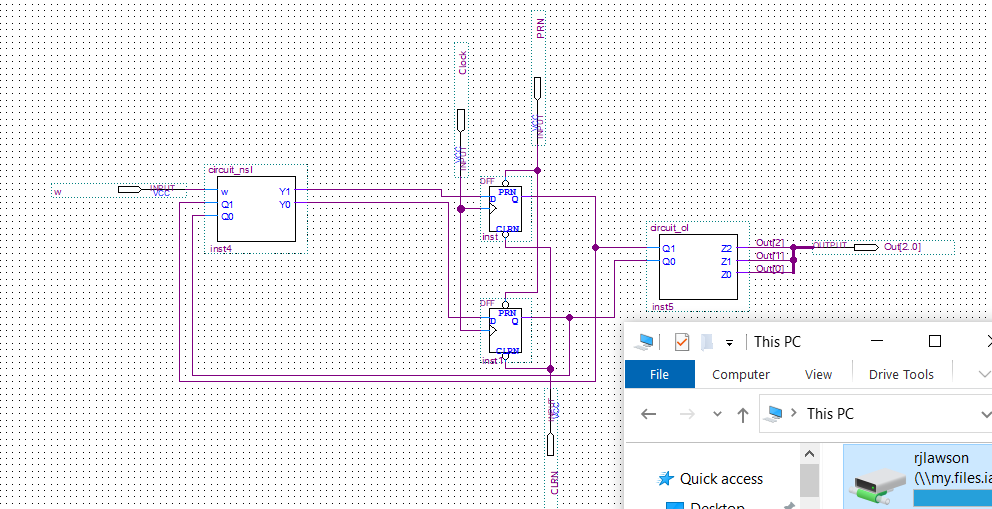
<<< Insert a screenshot of your waveform for your modulo-6 counter here>>>

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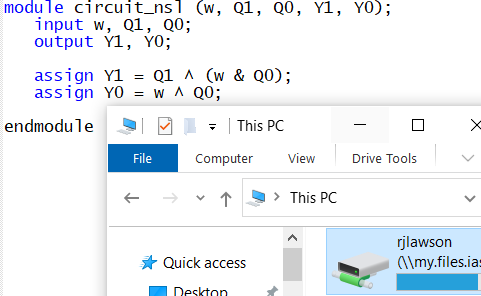
**3.0 A Simple Counter**

Screenshots:

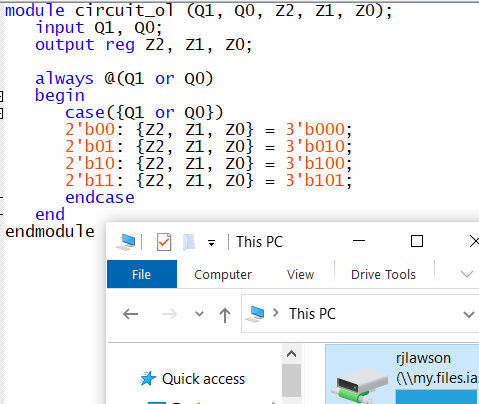
<<<Insert a screenshot of your simple counter here>>>



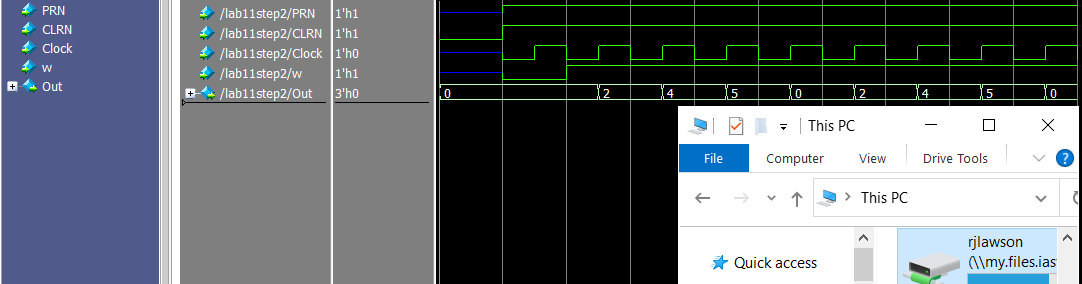
<<<Insert a screenshot of your next state logic here>>>



<<<Insert a screenshot of your output logic here>>>



<<< Insert a screenshot of your waveform for your simple counter here>>>

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